AMENDMENT TO THE CLAIMS

The claims in this listing will replace all prior claims in the application.

Listing of Claims:

1. (Canceled)

2. (Currently Amended): The circuit of claim ~~1~~ 3 wherein the voltage divider module further comprises a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter.

3. (Currently amended): A clock lock detection circuit comprising~~The circuit of claim 1~~;

a first input indicating an edge of a first clock;

a second input indicating a corresponding edge of a second clock wherein the second clock is expected to be synchronized with the first clock with an allowable time difference;

a difference generation module for generating a difference signal based on the time difference between the first and second inputs wherein the difference generation module is an XOR gate~~.~~; and

a voltage divider module for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs.

4. (Currently amended): The circuit of claim ~~1~~ 3 further comprising a voltage comparator for comparing the indication voltage against a predetermined threshold voltage for generating a

lock signal indicating whether the time difference is within the allowable time difference.

5. (Original): The circuit of claim 4 wherein the voltage comparator is a Schmitt trigger.

6. (Original): The circuit of claim 4 further comprising a buffer module passing the lock signal.

7. (Currently amended): A clock lock detection circuit comprising:

a first input indicating an edge of a first clock;

a second input indicating a corresponding edge of a second clock wherein the second clock is expected to be synchronized with the first clock with an allowable time difference;

a difference generation module for generating a difference signal based on the time difference between the first and second inputs;

a voltage divider module containing a capacitor for receiving the difference signal and generating an indication voltage which varies due to a charging and discharging process of the capacitor influenced by a change of the time difference between the first and second inputs; and

a voltage comparator for comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference is within the allowable time difference; and

a buffer module passing the lock signal.

8. (Original): The circuit of claim 7 wherein the voltage divider module has a CMOS

inverter and a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter.

9. (Original): The circuit of claim 7 wherein the difference generation module is an XOR gate.

10. (Original): The circuit of claim 7 wherein the voltage comparator is a Schmitt trigger.

11. (Canceled)

12. (Canceled)

13. (Currently amended): The method of claim ~~12~~ 14 wherein the voltage divider module further has a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter and, wherein the indication voltage is the output of the CMOS inverter.

14. (Currently amended): ~~The method of claim 12~~ A method for detecting whether two clock signals have an allowable time difference, the method comprising:

generating a first signal indicating an edge of a first clock;

generating a second signal indicating a corresponding edge of a second clock wherein the edge of the second clock is expected to be close to the edge of the first clock within the

allowable time difference;

generating a difference signal based on a time difference between the first and second signals, wherein the generating of a difference signal ~~further~~ includes feeding the first and second signals to an XOR gate ~~for generating the difference signal~~; and

generating an indication voltage which varies based on a change of the time difference between the first and second signals.

15. (Currently amended): The method of claim ~~12~~ 14 further comprising comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference between the first and second signals is within the allowable time difference.

16. (Previously presented): The method of claim 15 wherein the step of comparing the indication voltage against a predetermined threshold voltage further comprises feeding the indication voltage into a Schmitt trigger.

17. (Previously presented): The method of claim 15, further comprising passing the lock signal through a buffer module.

18. (Canceled)

19. (Currently amended): The circuit of claim ~~18~~ 20 wherein the voltage divider module has

a CMOS inverter and a capacitor wherein the inverter has first and second supply voltages with the capacitor connected to the second supply voltage and an output of the CMOS inverter.

20. (Original): A phase lock loop circuit comprising:~~The circuit of claim 18~~

a first flip-flop receiving a first clock and generating a first signal indicating an edge of the first clock;

a second flip-flop receiving a second clock and generating a second signal indicating a corresponding edge of the second clock wherein the edge of the second clock is expected to be close to the edge of the first clock within an allowable time difference;

a reset signal generator using the first and second signals to generate a reset signal for the first and second flip-flops;

a clock lock detection circuit comprising:

a difference generation module for generating a difference signal based on the time difference between the first and second signals, wherein the difference generation module is an XOR gate;

a voltage divider module containing a capacitor for receiving the difference signal and generating an indication voltage which varies due to a charging and discharging process of the capacitor influenced by a change of the time difference between the first and second signals; and

a voltage comparator for comparing the indication voltage against a predetermined threshold voltage for generating a lock signal indicating whether the time difference is within the allowable time difference.

21-24. (Canceled)

25. (New): A clock lock detection circuit comprising:

a first input indicating an edge of a first clock;

a second input indicating a corresponding edge of a second clock wherein the second clock is expected to be synchronized with the first clock with an allowable time difference;

a difference generation module for generating a difference signal based on the time difference between the first and second inputs;

a voltage divider module for receiving the difference signal and generating an indication voltage which varies based on a change of the time difference between the first and second inputs; and

a buffer module passing the lock signal.